Amendments to the Drawings

The attached proposed sheets of drawings include changes to Figs. 2 and 3 and replacement sheets replacing the original drawing sheets of Figs. 1 and 2 and Figs. 3 and 4A.

The changes involve the addition to Figs. 2 and 3 of a seed layer 35 between a metal body 36 and an adhesion/barrier layer 34 and the profile of the metal body 36, the seed layer 35, and the adhesion/barrier layer 34 for better clarity and for agreement with the references made in the Specification.

Attachment: Replacement sheets

REMARKS

The Examiner is thanked for the thorough examination and search of the subject patent application.

Claims 69-76 and 78-90 are pending; Claims 69 and 80 have been currently amended; Claims 1-68 and 77 have been canceled. No new matter is believed to have been added.

Please amend the Specification and the drawings for better clarity and for agreement with the references made in the Specification.

Response to Drawing Objection

Reconsideration of drawing objection under 37 CFR 1.83(a) as the following must be shown: a) gold seed layer (See Claim 69) and b) electroplated gold layer (See Claim 69) is respectfully requested.

Figs. 2 and 3 have been currently amended to show a gold seed layer 35 and an electroplated gold layer 36 on the gold seed layer 35. ~ *See Figs. 2 and 3 and the third paragraph of page 10, in the original specification* ~

Withdrawal of the drawing objection is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 112

Reconsiderations of Claim 80 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, are respectfully requested based on the following remarks.

Applicants teach that a gold layer 36 is connected to a copper pad 24 through an opening in a passivation layer 30. The gold layer 36 is connected through the gold seed layer 35, the barrier layer 34, and the metal cap layer 32 to the copper pad 24. ~ *See Fig. 2, the second paragraph of page 9 through the third paragraph of page 10, in the original specification* ~ The claimed subject matter that "said gold layer is connected to said copper pad through said opening in said passivation layer" is believed to comply with the written description requirement.

Withdrawal of Rejection under 35 U.S.C. 112, first paragraph, to Claim 80 is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 69-76, 78 and 79

As currently amended, independent claim 69 is recited below:

69. A semiconductor chip with a wirebonded wire, comprising:
a silicon substrate;
an active device in and on said silicon substrate;
a first dielectric layer over said silicon substrate;
an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;
a second dielectric layer between said first and second metal layers;
a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region;
an aluminum cap comprising a first portion directly over said first region and a second portion directly over said passivation layer, wherein said aluminum cap is connected to said copper pad through said opening in said passivation layer, and wherein said aluminum cap has a width greater than that of said opening in said passivation layer;
an adhesion/barrier layer on said aluminum cap; and
a gold layer on said adhesion/barrier layer and directly over said first and second portions of said aluminum cap, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said electroplated gold layer has a thickness between 2 and 20 micrometers, and wherein said wirebonded wire is joined with said gold layer.

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Reconsiderations of Claims 69-71 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Pat. No. 6,963,138) in view of Applicant's Prior Art and Raskin et al. (U.S. Pat. No. 6,878,633), of Claim 72 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Silicon Processing by Wolf et al., of Claims 73 and 74 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Microchip Fabrication by Peter Van Zant, of Claim 75 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Hashimoto (U.S. Pat. No. 6,255,737) and of Claim 79 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin

et al. and Lin (U.S. Pat. No. 6,383,916) are respectfully requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip claimed in amended Claim 69 patentably distinguishes over the citation by Low et al. (U.S. Pat. No. 6,963,138) in view of Applicant's Prior Art and Raskin et al. (U.S. Pat. No. 6,878,633).

The Examiner considers that "It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include an adhesion/barrier layer on said aluminum cap and a gold layer on said adhesion/barrier layer and directly over aluminum cap wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer and wherein said wirebonded wire is joined with said gold layer as disclosed in Raskin because it aids in providing a structure with a lower cost (For Example: See Avstract)." ~ *See lines 13-19 on page 5, in the last Office Action mailed Jun. 11, 2008* ~

Applicant respectfully traverses the Examiner's opinion because it would have not been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include Raskin et al.'s pad 6, 18 and 4 for being joined with a wirebonded wire. Raskin et al. teach that a gold layer 4 and a seed layer 6 and 18 of nickel-gold may be formed on an aluminum pad 14 and is used to have a solder bump 10 formed thereon. ~ *See Fig. 14 and col. 5, lines 31-36* ~ Even in the teaching of Low et al. in view of Raskin et al., those skilled in the art would come up with Raskin et al.'s gold layer 4 and seed layer 6 and 18 of

nickel-gold to be formed on an aluminum pad 14 in Low et al.'s device for a solder bumping process, but not for a wirebonding process because Raskin et al. fail to teach, hint or suggest that the gold layer 4 and the seed layer 6 and 18 of nickel-gold may have a wirebond formed thereon.

The Examiner considers that "The applicant has not established the critical nature of a "gold layer has a thickness of between about 2μm and 20μm." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims.....In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have various ranges." *~ See line 22 of page 5 through line 5 of page 6, in the last Office Action mailed Jun. 11, 2008 ~*

Applicant respectfully traverses the Examiner's opinion because it would have not been obvious to one having ordinary skill in the art at the time a gold layer was made to have a thickness between 2μm and 20μm. A gold layer having a thickness between 2μm and 20μm is critical for wirebonding. Thick gold, such as between 2μm and 20μm, is soft and compliant enough to absorb a wirebonding impact thereto, preventing circuit layers and dielectric layers thereunder from being damaged by the wirebonding impact, which is believed to be not anticipated by Low et al. and Raskin et al.

Withdrawal of the rejection to Claim 69 under 35 U.S.C. 103(a) is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-76, 78 and 79 patently define over the prior art as well.

Response to Claims 80-90

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As currently amended, independent claim 80 is recited below:

80. A semiconductor chip with a wirebonded wire, comprising:
a silicon substrate;
an active device in and on said silicon substrate;
a first dielectric layer over said silicon substrate;
an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;
a second dielectric layer between said first and second metal layers;
a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region;
an adhesion/barrier layer over said first region and over said passivation layer; and
a gold layer on said adhesion/barrier layer, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer, and wherein said wirebonded wire is joined with said gold layer.

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Reconsiderations of Claims 80-82 and 87-89 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. (U.S. Pat. No. 6,963,138) in view of Applicant's Prior Art and Raskin et al. (U.S. Pat. No. 6,878,633), of Claim 83 rejected under 35 U.S.C. 103(a) as being

unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Silicon Processing by Wolf et al., of Claims 84 and 85 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Microchip Fabrication by Peter Van Zant, of Claim 86 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Hashimoto (U.S. Pat. No. 6,255,737) and of Claim 90 rejected under 35 U.S.C. 103(a) as being unpatentable over Low et al. in view of Applicant's Prior Art, Raskin et al. and Lin (U.S. Pat. No. 6,383,916) are respectfully requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip claimed in amended Claim 80 patentably distinguishes over the citation by Low et al. (U.S. Pat. No. 6,963,138) in view of Applicant's Prior Art and Raskin et al. (U.S. Pat. No. 6,878,633).

The Examiner considers that "It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include a gold layer on said adhesion/barrier layer, wherein said gold layer comprises a gold seed layer and an electroplated gold layer on said gold seed layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer and wherein said wire is joined with said gold layer as disclosed in Raskin because it aids in providing a structure with a lower cost (For Example: See Avstract)." ~ *See lines 13-21 on page 9, in the last Office Action mailed Jun. 11, 2008* ~

Applicant respectfully traverses the Examiner's opinion because it would have not been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Low to include Raskin et al.'s pad 6, 18 and 4 for being joined with a wirebonded wire. Raskin et al. teach that a gold layer 4 and a seed layer 6 and 18 of nickel-gold may be formed on an aluminum pad 14 and is used to have a solder bump 10 formed thereon. ~ *See Fig. 14 and col. 5, lines 31-36* ~ Even in the teaching of Low et al. in view of Raskin et al., those skilled in the art would come up with Raskin et al.'s gold layer 4 and seed layer 6 and 18 of nickel-gold to be formed on an aluminum pad 14 in Low et al.'s device for a solder bumping process, but not for a wirebonding process because Raskin et al. fail to teach, hint or suggest that the gold layer 4 and the seed layer 6 and 18 of nickel-gold may have a wirebond formed thereon.

Withdrawal of the rejection to Claim 80 under 35 U.S.C. 103(a) is respectfully requested.

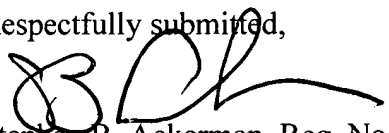
For at least the foregoing reasons, applicants respectfully submit independent claim 80 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 81-90 patently define over the prior art as well.

Conclusion

All of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Lewis not find that the Claims are now Allowable that she call the undersigned at 845 452-3204 to overcome any problems preventing allowance.

Respectfully submitted,



Stephen B. Ackerman, Reg. No. 37,761

Attachment: Replacement sheets